App. Serial No 10/524,981
Docket No.: NL030866 US

In the claims:

Please amend claims 16 and 19, and add new claims 25-31 as indicated below. This listing of claims replaces all prior versions.

1-15. (*Cancelled*)

16. (*Currently Amended*) A method of manufacturing a ferroelectric device

wherein a body is formed that comprises a substrate, and the device is provided with a ferroelectric layer having a connection conductor on a side facing away from the substrate,

an oxygen-free ferroelectric material being selected as the material for the ferroelectric layer which is used to form an active electrical element,

forming a field effect transistor in the substrate, the field effect transistor having a source region, a drain region and a gate electrode,

applying a barrier layer directly to the source region or the drain region,

applying a conductive layer directly to the barrier layer, characterized in that [[a]] the conductive layer is provided between the substrate and the ferroelectric layer, and the ~~which~~ conductive layer forms a further connection conductor of the ferroelectric layer, and

the ~~memory~~ active electrical element is obtained by forming a Schottky junction between the ferroelectric layer and at least one of the connection conductors.

17. (*Previously Presented*) A method according to claim 16, characterized in that the active electrical element is formed as a memory element.

18. (*Previously Presented*) A method as claimed in claim 17, characterized in that the body is formed so as to be a semiconductor body, and a semiconductor substrate is selected as the substrate.

19. (*Currently Amended*) A method as claimed in claim 17, characterized in that ~~in the semiconductor body there is formed a field effect transistor with a source~~ region, ~~a drain~~

~~region and a gate electrode, and~~ the further connection conductor ~~is provided on the source or drain region of the field effect transistor and~~ is formed so as to be a connection conductor of the source region or drain region.

20. (*Previously Presented*) A method as claimed in claim 17, characterized in that the Schottky junction is formed between the further connection conductor and the ferroelectric layer, and an ohmic contact is formed between the connection conductor and the ferroelectric layer as well as between the further connection conductor and the source or drain region of the field effect transistor.

21. (*Previously Presented*) A method as claimed in claim 17, characterized in that the ferroelectric layer is formed by converting part of a conductive layer to the ferroelectric material, one of the connection conductors being formed by the remaining part of the conductive layer.

22. (*Previously Presented*) A method as claimed in claim 17, characterized in that a matrix of N x M memory elements is formed, where N and M are natural numbers and each memory element is provided on both sides with an electric connection.

23. (*Previously Presented*) A method as claimed in claim 22, characterized in that each memory element is coupled to a field effect transistor formed in the device and associated with said memory element, which field effect transistor comprises a source region, a drain region and a gate electrode, and the device is provided with N first conductor tracks, M second conductor tracks and with a ground connection, and each memory element is connected via the connection conductor to one of the N first conductor tracks and via the further connection conductor to the source or drain region of the associated field effect transistor, of which the other drain or source region is connected to the ground connection, while the gate electrode is connected to one of the M second conductor tracks.

24. (*Cancelled*)

25. (*New*) A method of manufacturing a ferroelectric device

wherein a body is formed that comprises a substrate, and the device is provided with a ferroelectric layer having a connection conductor on a side facing away from the substrate,

an oxygen-free ferroelectric material being selected as the material for the ferroelectric layer which is used to form an active electrical element, characterized in that a conductive layer is provided between the substrate and the ferroelectric layer, and the conductive layer forms a further connection conductor of the ferroelectric layer, and

the active electrical element is obtained by forming a Schottky junction between the ferroelectric layer and at least one of the connection conductors, and

characterized in that the ferroelectric layer is formed by converting part of a conductive layer to the ferroelectric material, one of the connection conductors being formed by the remaining part of the conductive layer.

26. (*New*) A method according to claim 25, characterized in that the active electrical element is formed as a memory element.

27. (*New*) A method as claimed in claim 26, characterized in that the body is formed so as to be a semiconductor body, and a semiconductor substrate is selected as the substrate.

28. (*New*) A method as claimed in claim 26, characterized in that in the semiconductor body there is formed a field effect transistor with a source region, a drain region and a gate electrode, and the further connection conductor is provided on the source or drain region of the field effect transistor and is formed so as to be a connection conductor of the source region or drain region.

29. (*New*) A method as claimed in claim 28, characterized in that the Schottky junction is formed between the further connection conductor and the ferroelectric layer, and an ohmic contact is formed between the connection conductor and the ferroelectric layer as

well as between the further connection conductor and the source or drain region of the field effect transistor.

30. (*New*) A method as claimed in claim 25, characterized in that a matrix of N x M memory elements is formed, where N and M are natural numbers and each memory element is provided on both sides with an electric connection.

31. (*New*) A method as claimed in claim 30, characterized in that each memory element is coupled to a field effect transistor formed in the device and associated with said memory element, which field effect transistor comprises a source region, a drain region and a gate electrode, and the device is provided with N first conductor tracks, M second conductor tracks and with a ground connection, and each memory element is connected via the connection conductor to one of the N first conductor tracks and via the further connection conductor to the source or drain region of the associated field effect transistor, of which the other drain or source region is connected to the ground connection, while the gate electrode is connected to one of the M second conductor tracks.